Figure 1

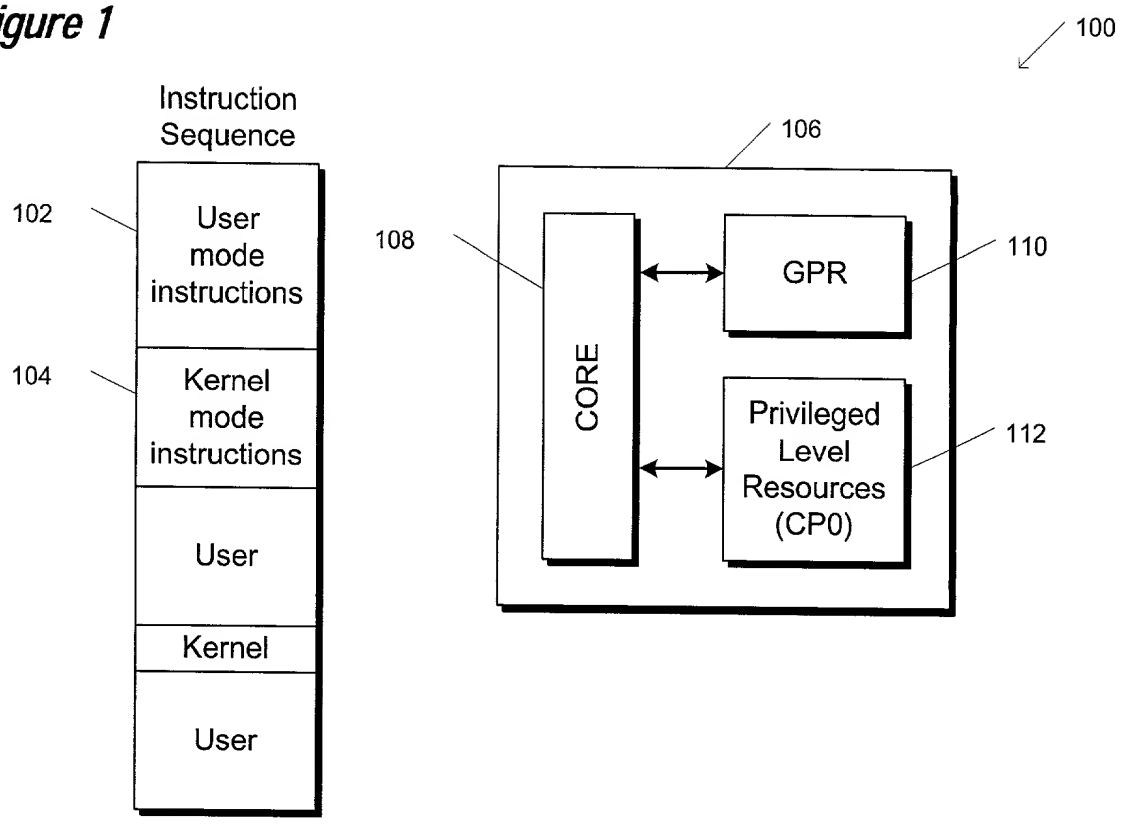

Figure 2

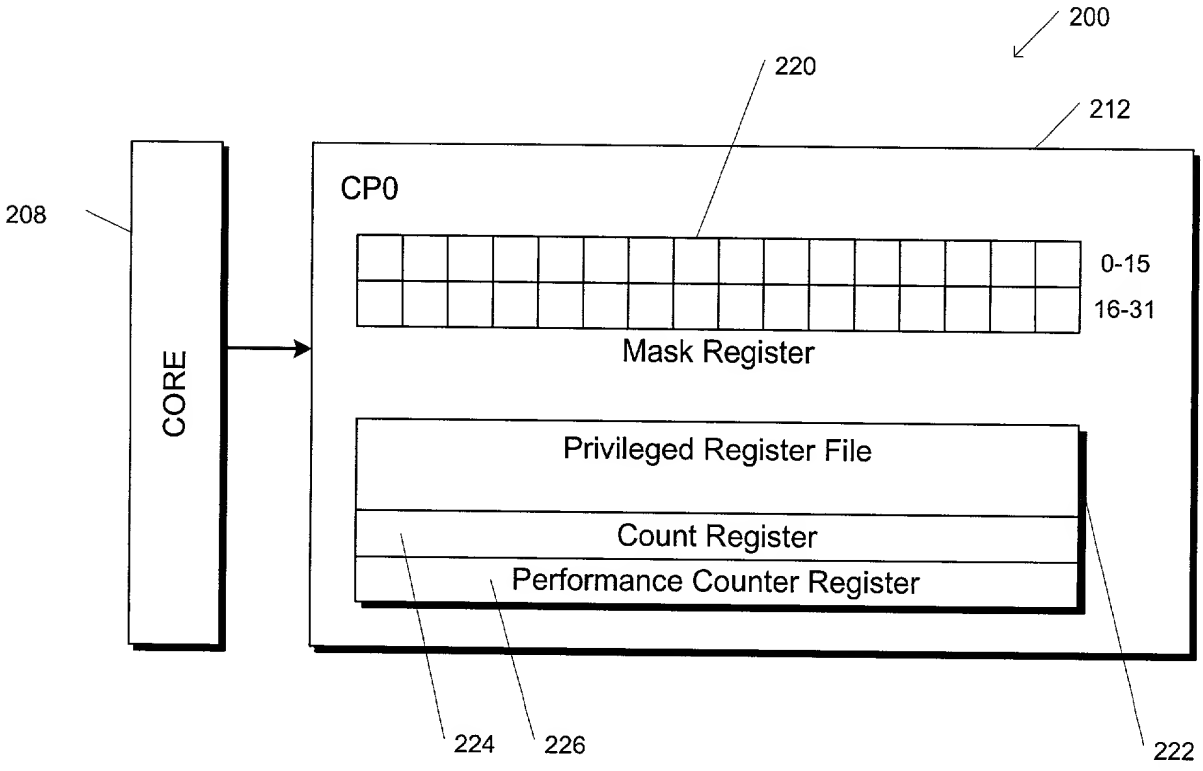

Figure 3

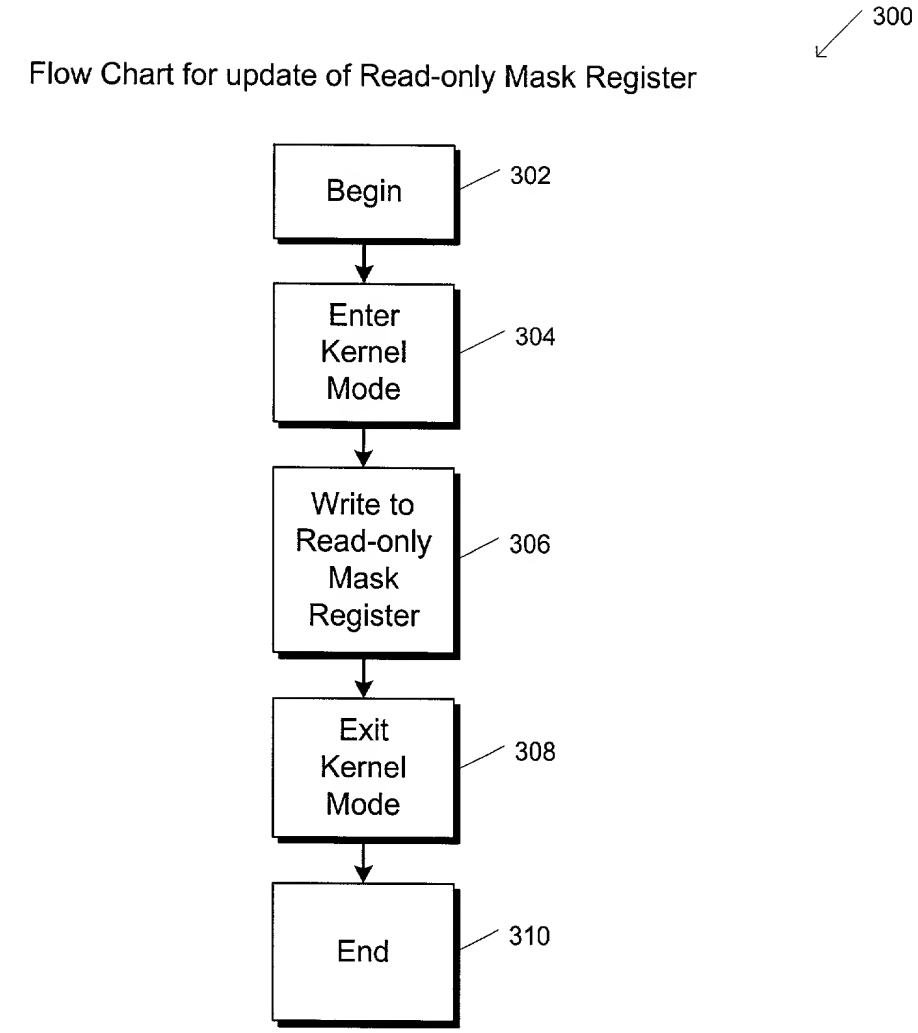
300
Flow Chart for update of Read-only Mask Register
Begin
302
Enter Kernel Mode
304
Write to Read-only Mask Register
306
Exit Kernel Mode
308
End
310

Figure 4

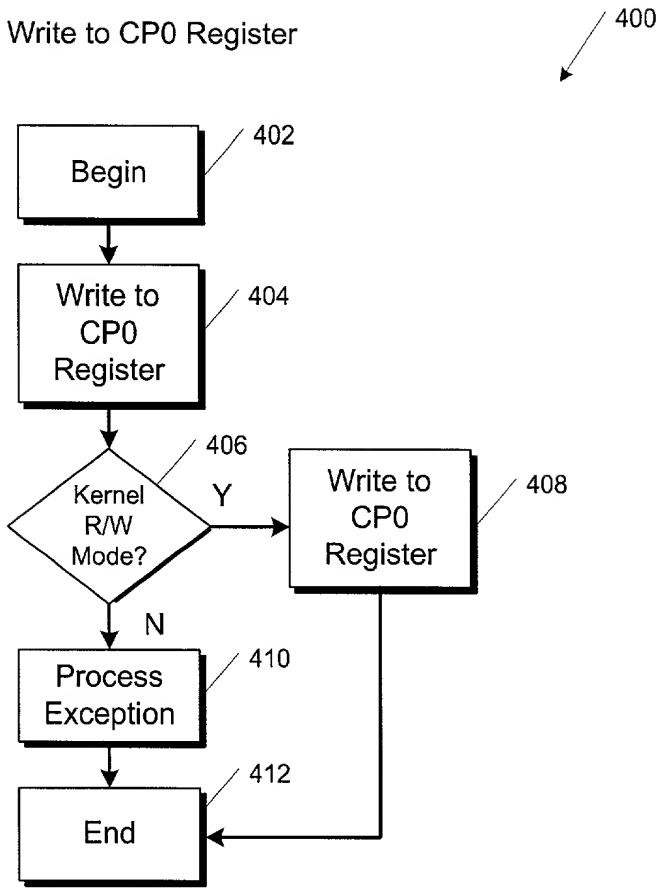
Write to CP0 Register
400
Begin
402
Write to CP0 Register
404
Kernel R/W Mode?
406
Y
Write to CP0 Register
408
N
Process Exception
410
End
412

Figure 5

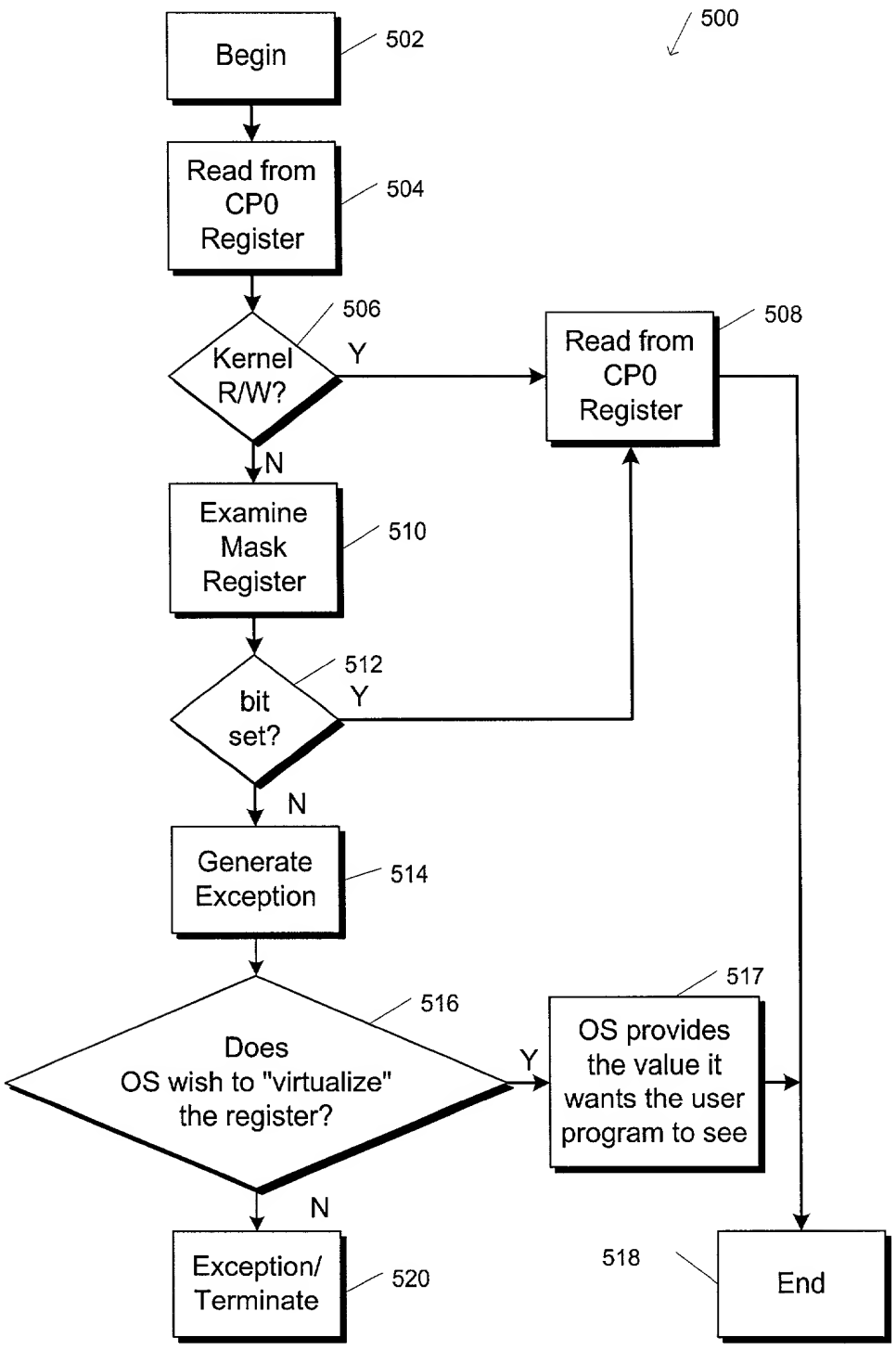
Read from CP0 Register
500
Begin
502
Read from CP0 Register
504
Kernel R/W?
506
Y
N
Read from CP0 Register
508
Examine Mask Register
510
bit set?
512
Y
N
Generate Exception
514
Does OS wish to "virtualize" the register?
516
Y
N
OS provides the value it wants the user program to see
517
Exception/ Terminate
520
End
518

Figure 6

600

Mnemonic	Function
RDC0	Move from Coprocessor Zero (Read-only)
DRDC0	Doubleword Move from CP0 (Read-only)
MTC0	Move to CPO bit mask (Kernel Mode only)